REMARKS

The present Amendment cancels claims 2-8 and 17, and leaves claim 1 unchanged. Therefore, the present application has pending claim 1.

35 U.S.C. §102 Rejections

Claims 1, 3-5 and 17 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 5,978,844 to Tsuchiya et al. ("Tsuchiya"). As previously indicated, claims 3-5 and 17 were canceled. Therefore, this rejection regarding claims 3-5 and 17 is rendered moot. This rejection regarding the remaining claim 1 is traversed for the following reasons. Applicants submit that the features of the present invention as now more clearly recited in claim 1 are not taught or suggested by Tsuchiya, whether taken individually or in combination with any of the other references of record. Therefore, Applicants respectfully request the Examiner to reconsider and withdraw this rejection.

Features of the present invention are clearly recited in the pending claim. Specifically, claim 1 clearly recites that the present invention is directed to a decentralized control system.

The present invention, as recited in claim 1, provides a decentralized control system. The control system includes a plurality of processors; a plurality of devices controlled by the plurality of processors; and at least one information transmission path for communicating control information between the plurality of processors and for communicating input/output information between the plurality of processors and the devices.

According to the present invention, each of the plurality of processors includes a processor detecting means. The processor detecting means detects a connection state of each of the plurality of processors with respect to the information

transmission path, where the connection state shows which processors of the plurality of processors are connected for controlling the plurality of devices, and is represented by an ID of each of the processors.

Also according to the present invention, the processor detecting means generates a list of available processors. At least one of the plurality of processors includes a program block assigning means and a program storage means. The program block assigning means assigns, based on the detected connection state detected by the processor detecting means, a plurality of mutually concurrently executable program blocks to control the device to each of the plurality of processors, respectively. The assigning means divides a program for controlling the devices into the mutually concurrently executable plurality of blocks allowing uniform assignment of a processing load to the processors in accordance with an average number of execution steps or an average processing time for one cycle of each of the plurality of program blocks. The assigning means also generates an assignment list, and distributes the assignment list and the mutually concurrently executable plurality of blocks to the processors.

The program storage means stores a relevant one of the plurality of mutually concurrently executable program blocks at each of the plurality of processors, where each of the plurality of processors executes the stored relevant program blocks, respectively. According to the present invention, each of the plurality of processors distributes the mutually concurrently executable plurality of blocks and the assignment list, and executes the program blocks based on the assignment list. The prior art does not teach or suggest all of these features.

The above described features of the present invention, as now more clearly recited in the claims, are not taught or suggested by any of the references of record,

particularly Tsuchiya, whether taken individually or in combination with any of the other references of record.

Tsuchiya teaches an internetworking apparatus for load balancing plural networks. However, there is no teaching or suggestion in Tsuchiya of the decentralized control system as recited in claim 1 of the present invention.

Tsuchiya discloses an internetworking apparatus for interconnecting a plurality of networks, having forwarding sections corresponding to interfaces of the networks, each including a processor for performing packet forwarding processing and a statistics unit for collecting processing time statistics of the processor. An adjusting section connected to all the forwarding sections through a bus instructs each processor to change a program to be executed thereby, based on the processing time statistics reported by each processor so as to balance processing loads on the respective processors.

Features of the present invention, as recited in claim 1, include where at least one of the plurality of processors includes: program block assigning means for assigning, based on the detected connection state detected by the processor detecting means, a plurality of mutually concurrently executable program blocks to control the device to each of the plurality of processors, respectively, where the program block assigning means divides a program for controlling the devices into the mutually concurrently executable plurality of blocks allowing uniform assignment of a processing load to the processors in accordance with an average number of execution steps or an average processing time for one cycle of each of the plurality of program blocks, generates an assignment list, and distributes the assignment list and the mutually concurrently executable plurality of blocks to the processors; and program storage means for storing a relevant one of the plurality of mutually

concurrently executable program blocks at each of the plurality of processors, each of the plurality of processors executing the stored relevant program blocks, respectively, and where each of the plurality of processors distributes the mutually concurrently executable plurality of blocks and the assignment list, and executes the program blocks based on the assignment list. Tsuchiya does not disclose this combination of features.

In the present invention, each of the processors within a network is individually arranged so as to allocate program blocks. Accordingly, it is possible to improve the reliability or flexibility of the system. Tsuchiya does not teach this feature.

To support the assertion that Tsuchiya teaches the claimed features, the Examiner asserts that Fig. 1, items 40-43 correspond to the program block assigning means, and that Fig. 1, element 82 corresponds to the features executed by the program block assigning means. However, neither of the cited elements, the accompanying text, nor any other portion of Tsuchiya, teaches or suggests the claimed features.

In Tsuchiya, each of the processors is not individually arranged so as to allocate program blocks. As shown in Fig. 1, and as described in column 3, lines 62-67, a single element, that is the "adjusting section 25", controls the so-called load allocation for each of the processors in the network (see, e.g., column 8, lines 42-30). This is quite different from the present invention.

Therefore, Tsuchiya fails to teach or suggest "wherein at least one of said plurality of processors comprises: program block assigning means for assigning, based on the detected connection state detected by said processor detecting means, a plurality of mutually concurrently executable program blocks to control the

device to each of said plurality of processors, respectively, wherein said program block assigning means divides a program for controlling said devices into said mutually concurrently executable plurality of blocks allowing uniform assignment of a processing load to the processors in accordance with an average number of execution steps or an average processing time for one cycle of each of the plurality of program blocks, generates an assignment list, and distributes the assignment list and said mutually concurrently executable plurality of blocks to said processors; and program storage means for storing a relevant one of the plurality of mutually concurrently executable program blocks at each of said plurality of processors, each of said plurality of processors executing the stored relevant program blocks, respectively," and "wherein each of said plurality of processors distributes said mutually concurrently executable plurality of blocks and said assignment list, and executes the program blocks based on said assignment list" as recited in claim 1.

Therefore, Tsuchiya does not teach or suggest the features of the present invention, as recited in claim 1. Accordingly, reconsideration and withdrawal of the 35 U.S.C. §102(e) rejection of claim 1 as being anticipated by Tsuchiya are respectfully requested.

The remaining references of record have been studied. Applicants submit that they do not supply any of the deficiencies noted above with respect to the references used in the rejection of claim 1.

35 U.S.C. §103 Rejections

Claims 2 and 8 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Tsuchiya in view of U.S. Patent No. 5,592,671 to Hirayama. As

previously indicated, claims 2 and 8 were canceled. Therefore, this rejection regarding claims 2 and 8 is rendered moot.

In view of the foregoing amendments and remarks, Applicants submit that claim 1 is in condition for allowance. Accordingly, early allowance of claim 1 is respectfully requested.

To the extent necessary, the applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any overpayment of fees, to the deposit account of MATTINGLY, STANGER, MALUR & BRUNDIDGE, P.C., Deposit Account No. 50-1417 (referencing Attorney Docket No. 500.37600CX1).

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